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Progress in the Contactless Capacitive Characterization of Semi-Insulating Substrates

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Outlay

- **Objective**
- **Basics of COntactless REsistivity MApping**
- **Technical Details**
  - COREMA – WT
  - COREMA – RM
  - COREMA – VT
- **Measurements**
  - Resistivity topography
  - Contactless mobility
  - Activation energy
- **Summary**

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Objective

To provide innovative analytic tools for

- **absolute**
- **rapid**
- **laterally resolved**
- **nondestructive**
- **precise**
- **low cost**

Evaluation of the electrical properties of compound semiconductor substrates for

- **production control**
- **material development**

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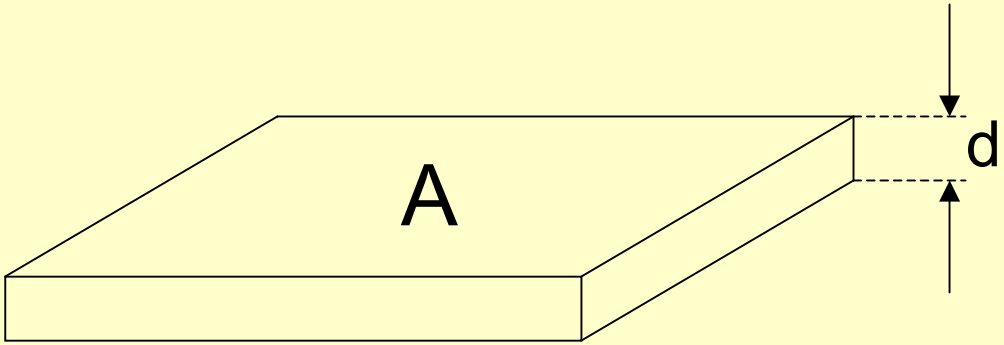
Basics of COntactless REsistivity MApping (I)



$$R_s = \rho\, d/A$$

$$C_s = \varepsilon\, A/d$$

$$R_s C_s = \rho\, \varepsilon = \tau$$

Semi-insulating semiconductor

$$\rho = \tau / \varepsilon$$

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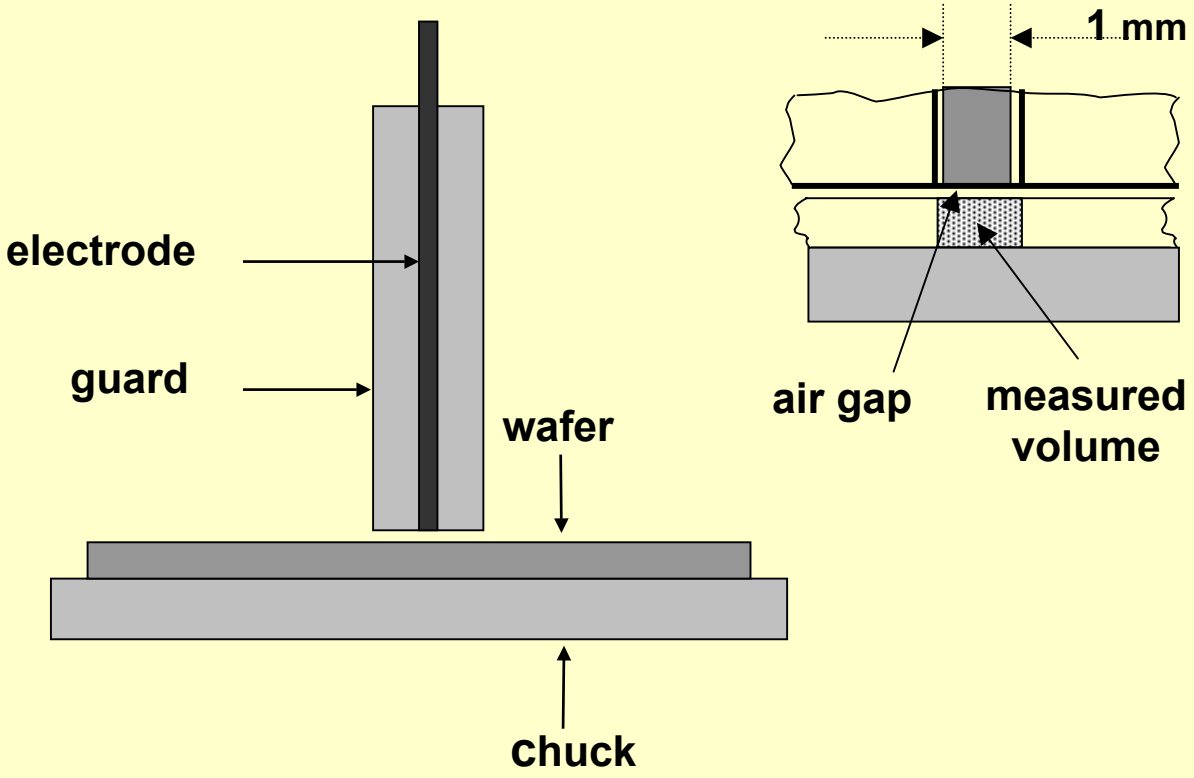
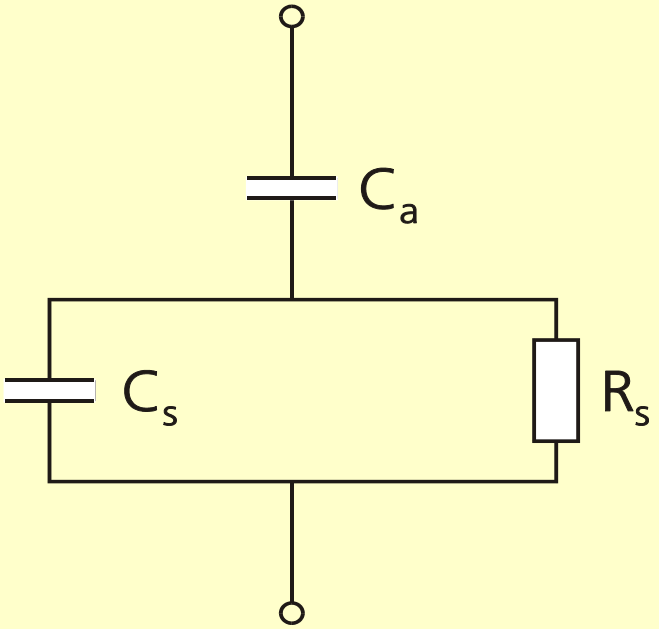
Basics of COntactless REsistivity MApping (II)

Capacitive probe



Equivalent circuit



$$\tau = R_s(C_s+C_a)$$

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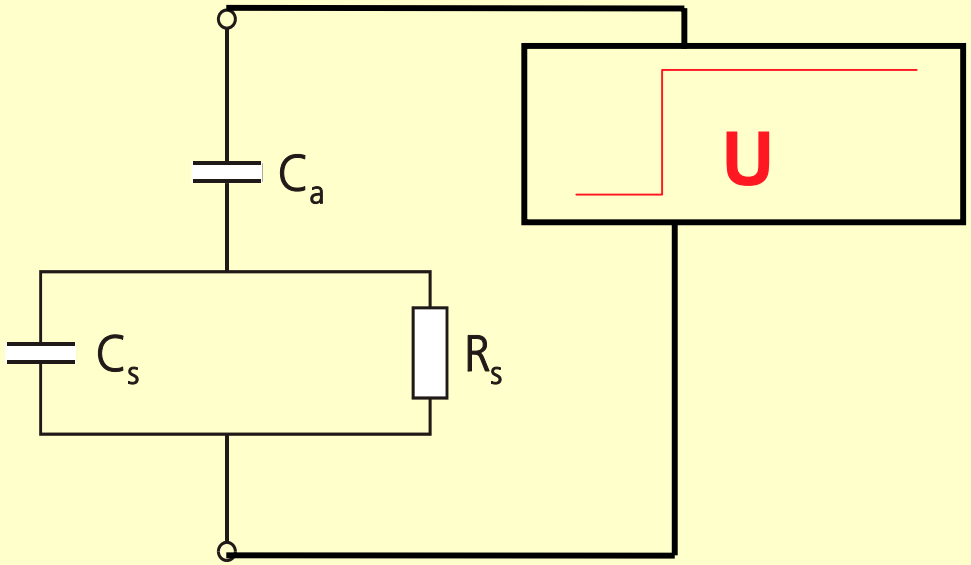
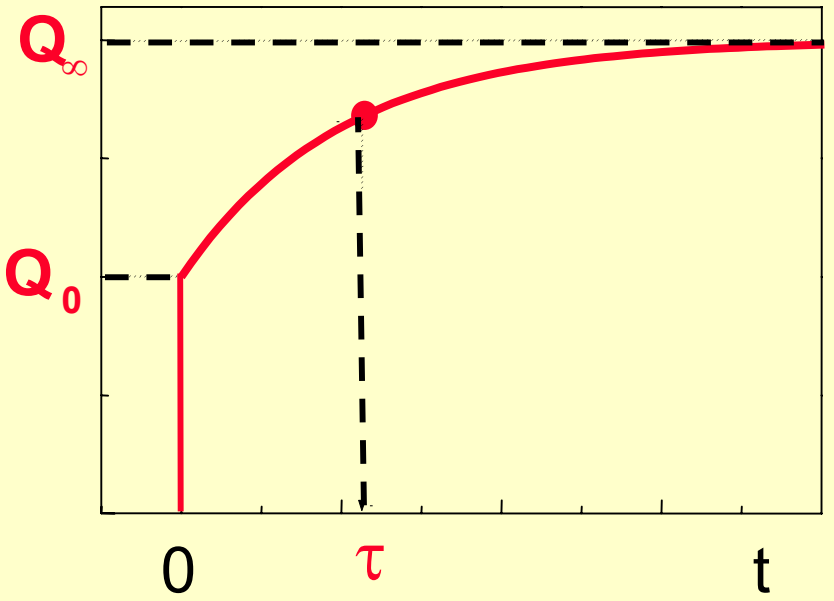
Basics of COntactless REsistivity MApping (III)

Equivalent circuit



Charge transient after voltage step application



$$\tau = R_s(C_s+C_a)$$

$$\rho = Q_0\,\tau\,(Q_\infty\,\varepsilon\,\varepsilon_0)^{-1}$$

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Basics of COntactless REsistivity MApping (IV)

Evaluation of electrical material properties

Resistivity	$\rho = Q_0\ \tau\ (Q_\infty\ \varepsilon\ \varepsilon_0)^{-1}$
Mobility	$\mu = 1/B\ [\ \rho(B) / \rho(0) - 1]^{1/2}$
Activation energy	$E_a = (kT_1T_2)/(T_2-T_1) * \ln [\rho(T_1) / \rho(T_2)]$

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Technical Details (I) COREMA - WT

Specifications

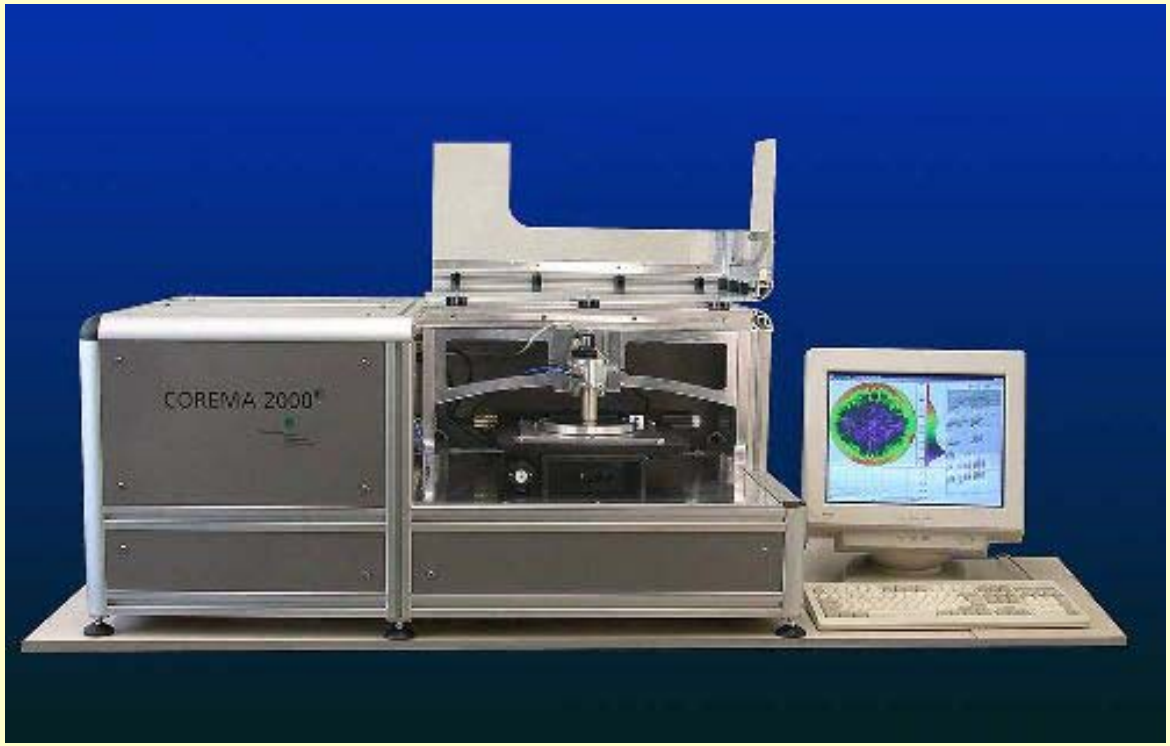
Range $1x10^5 – 1x10^{12}$ Ωcm

Wafer ∅ ≤ 200 mm

Probe ∅ ≤ 1 mm

Repeatability 1%

Speed 100 ms @ 1E7 Ωcm



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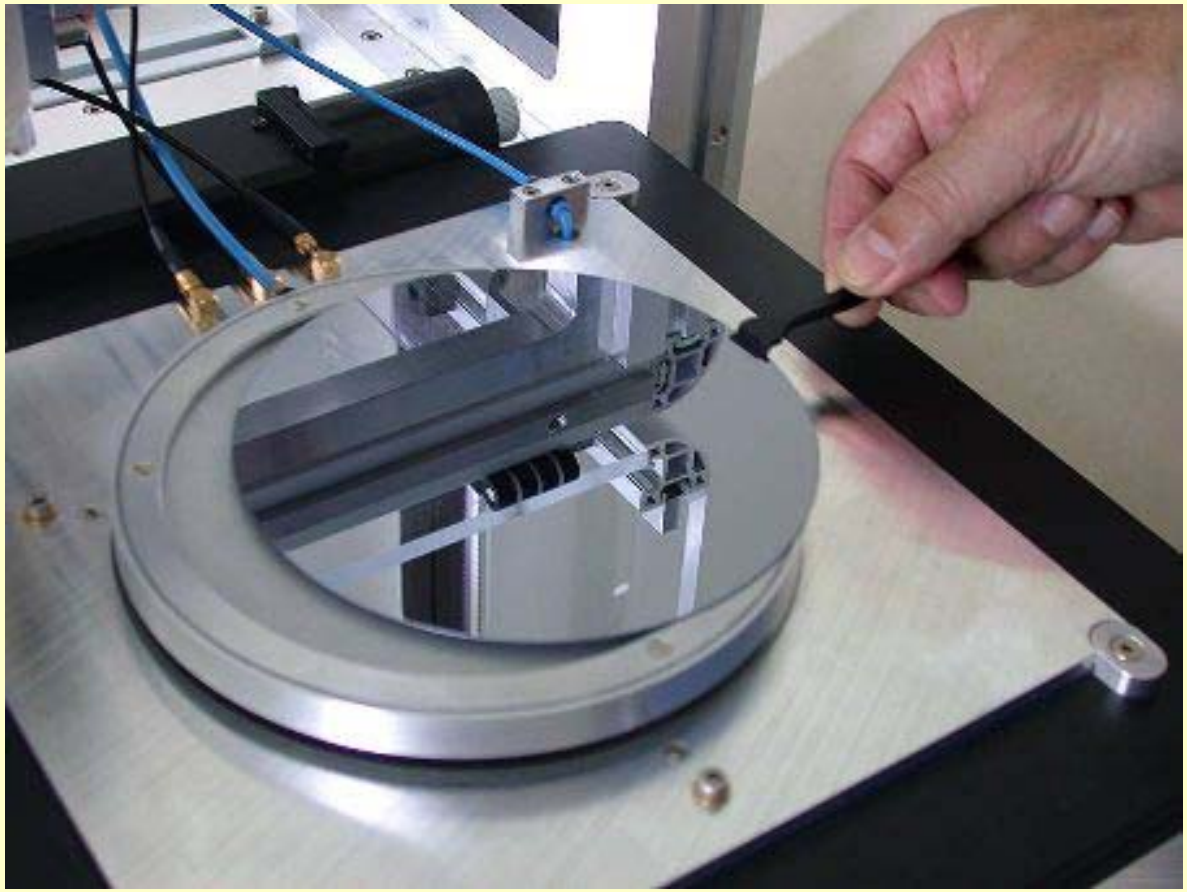
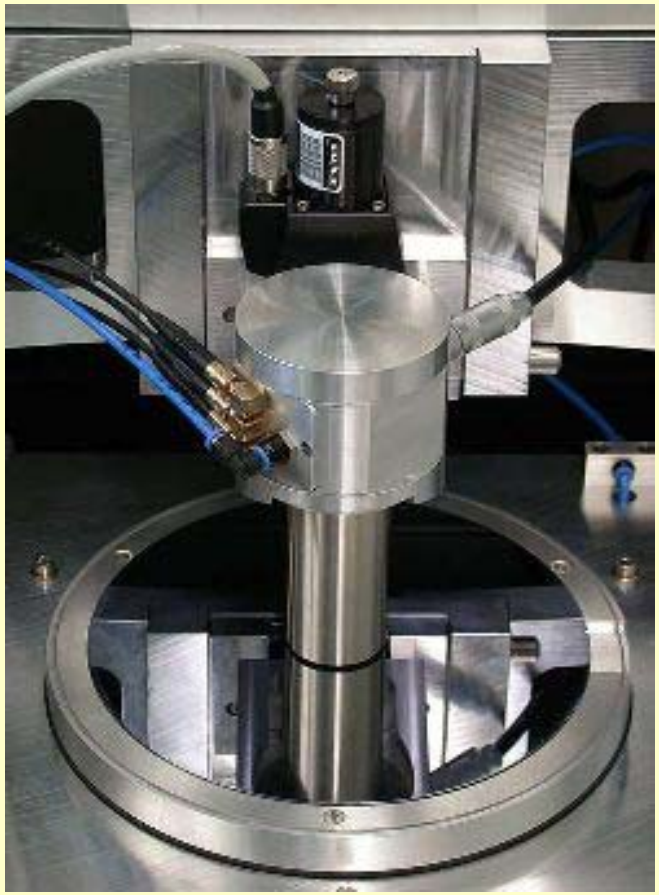
Technical Details (II) COREMA - WT





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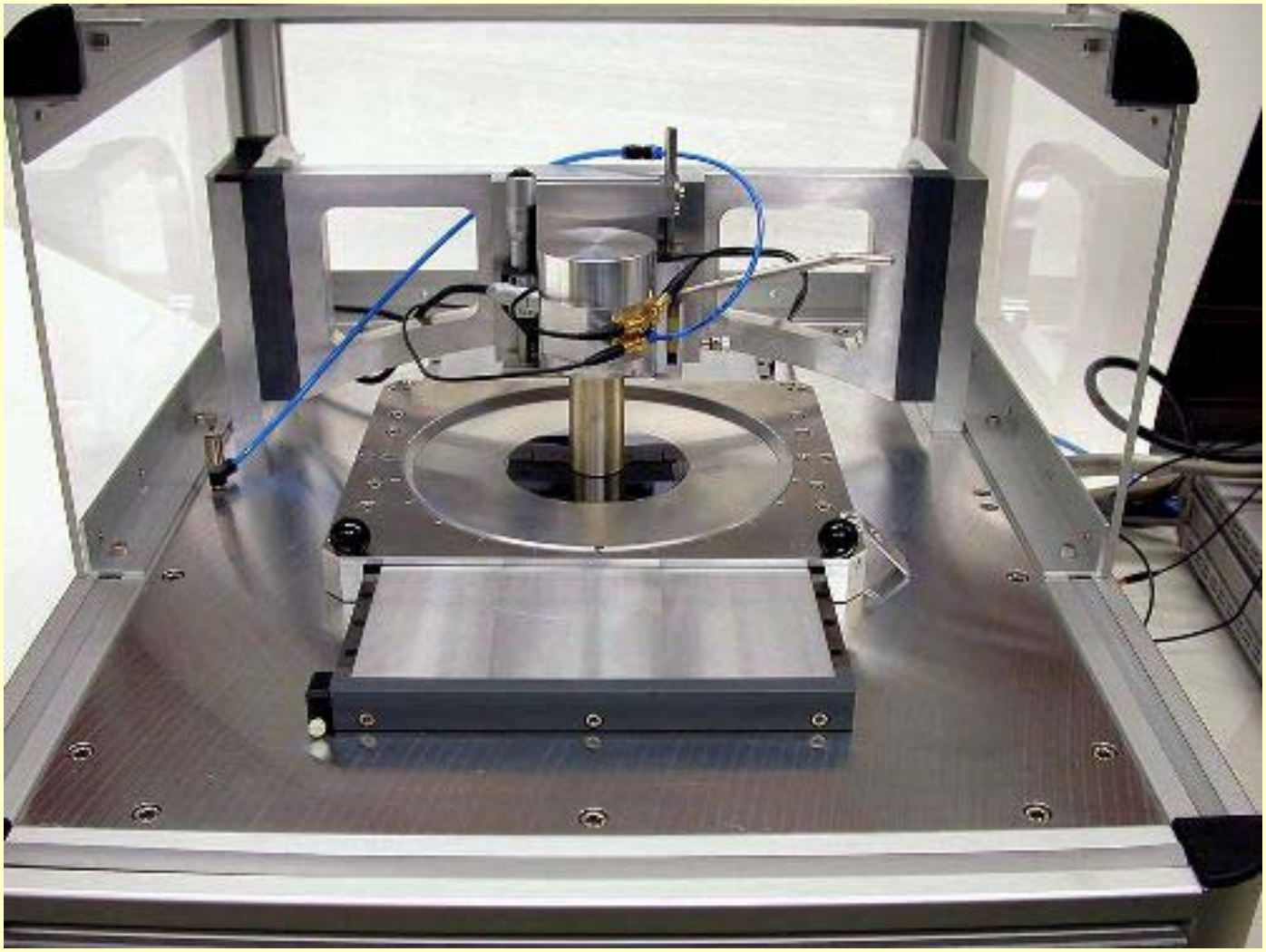
Technical Details (III) COREMA - RM



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Technical Details (IV) COREMA - VT

System designed to evaluate resistivity at Variable Temperature

- **Temperature range 300 K – 650 K**
- **Resisitvity range 2 x 10^{5} – 2 x 10^{11} Ωcm**
- **High temperature capacitive probe design**
- **Probe diameter 8 mm**
- **Sample diameter 10 mm – 100 mm**
- **Manual loading**
- **Free choice of measurement position**

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Resistivity Topography (I)

GaAs Substrate Production Control

150 mm GaAs wafer

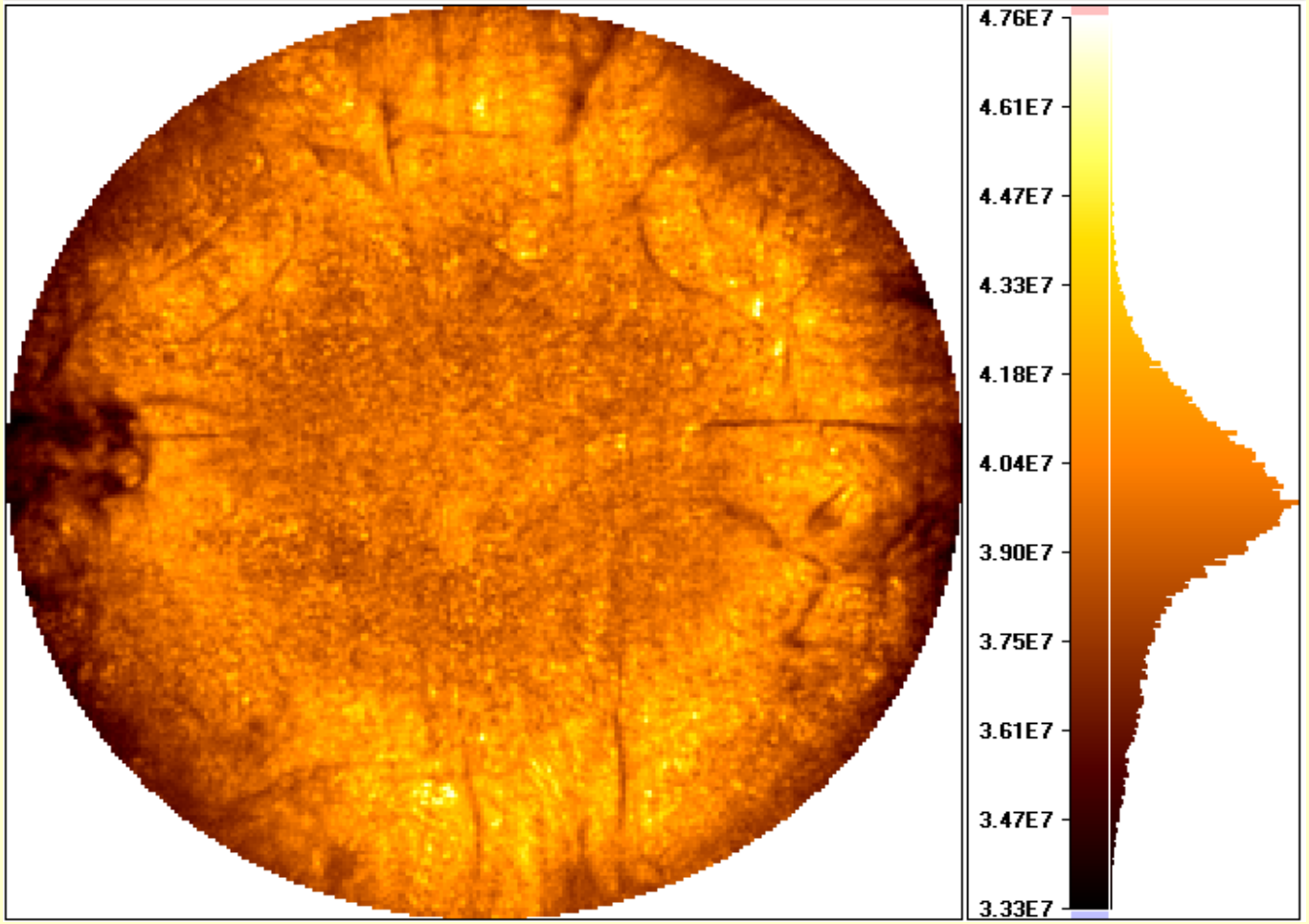
Mean: 3.96x10^7 Ω cm

Stdv: 4.27 %

Radial variation

Fourfold symmetry

Dislocation network



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Resistivity Topography (II)

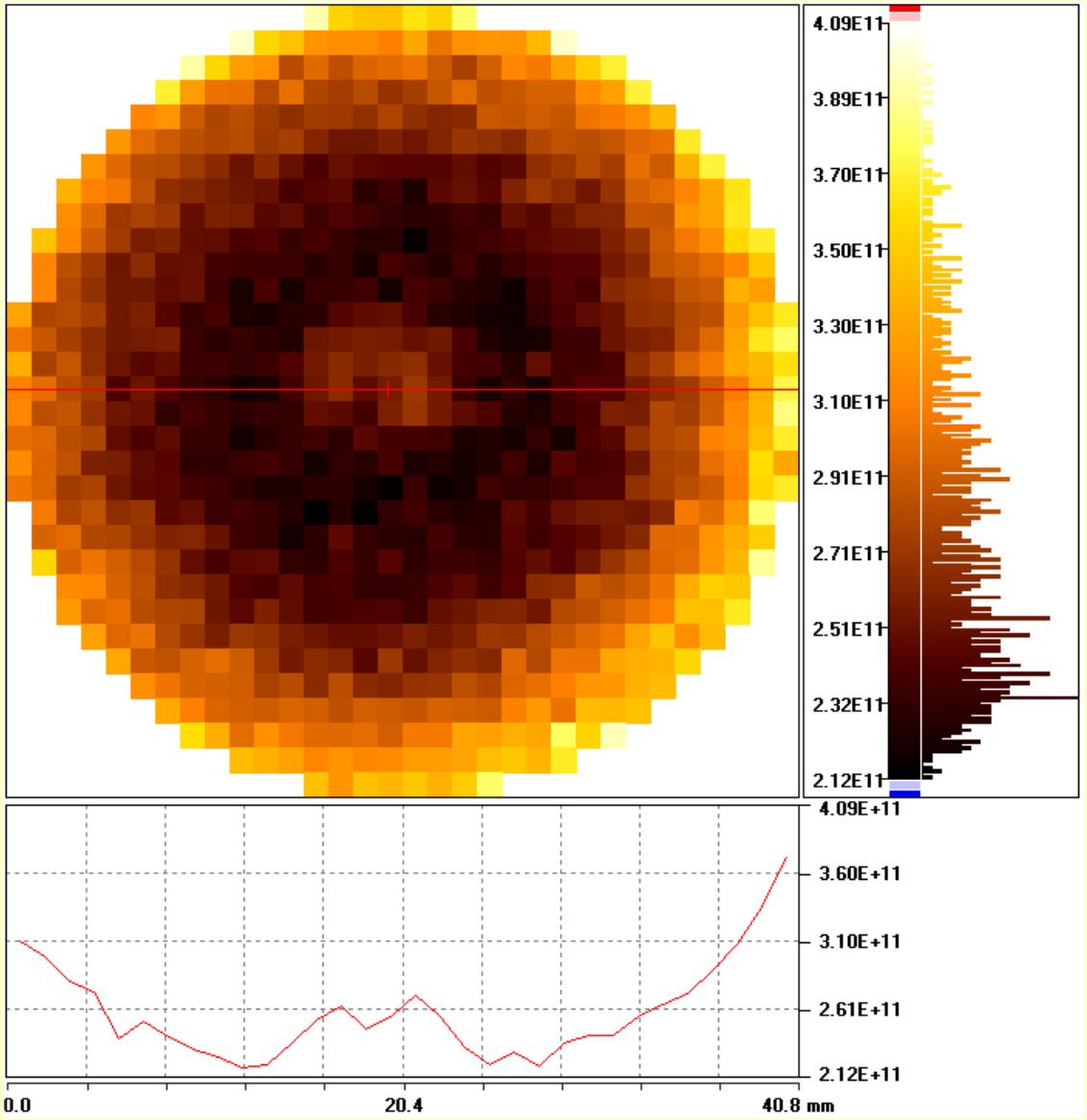
SiC Substrate Production Control

2“ SiC Wafer

2.12 x10^{11} - 4.09 x10^{11} Ωcm

Mean: 2.75 x10^{11} Ωcm

Stdv: 14.7%



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Resistivity Topography (III)

Exploratory SiC Material Development

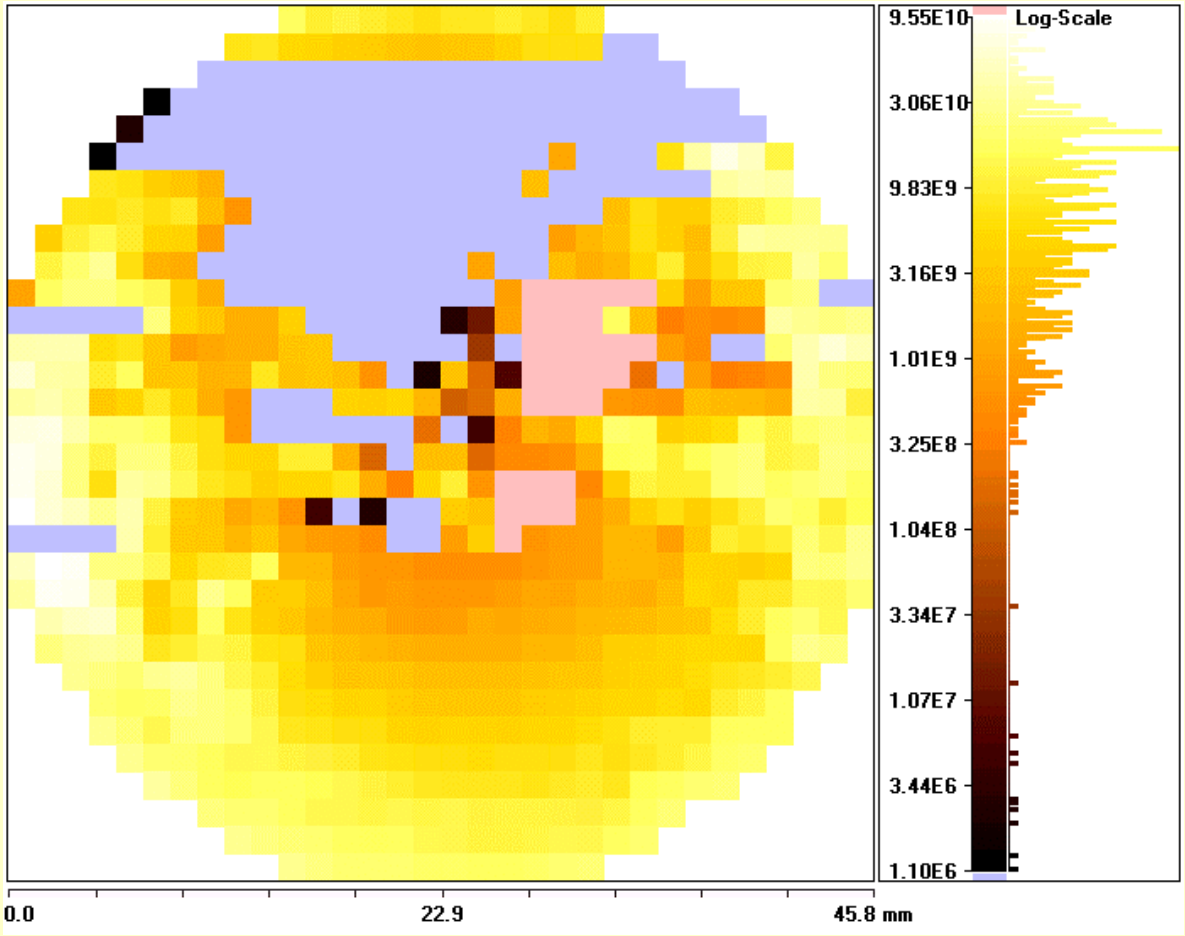
2“ SiC wafer

1.1 x10^6 – 1.0 x 10^{11} Ωcm

Blue area below 10^5 Ωcm

Pink area above 10^{12} Ωcm

Rapid order-of-magnitude fluctuations



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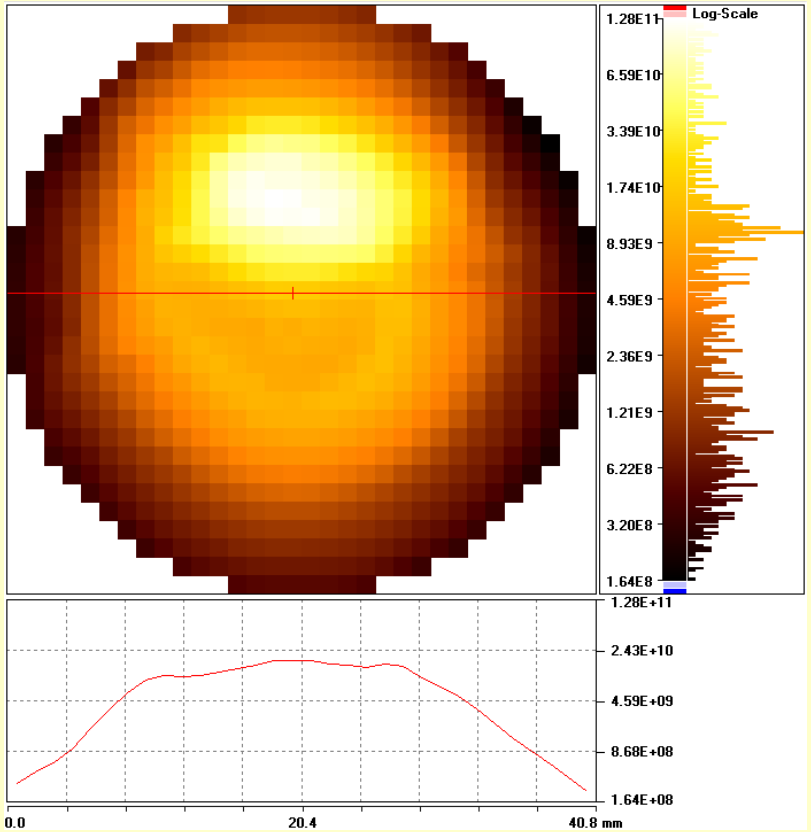
Resistivity Topography (IV)

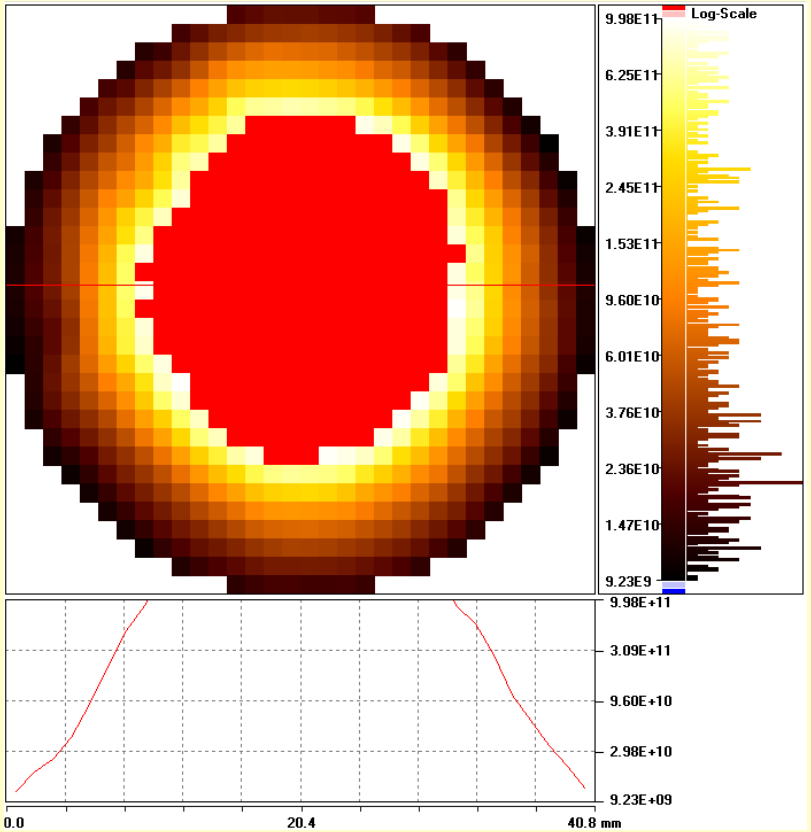
Analysis of Persistent Photoconductivity

Resistivity after 3h storage in darkness



Mean: 1.12 x10^{10} Ωcm

Resistivity after 48h storage in darkness



Mean: 1.65 x10^{11} Ωcm

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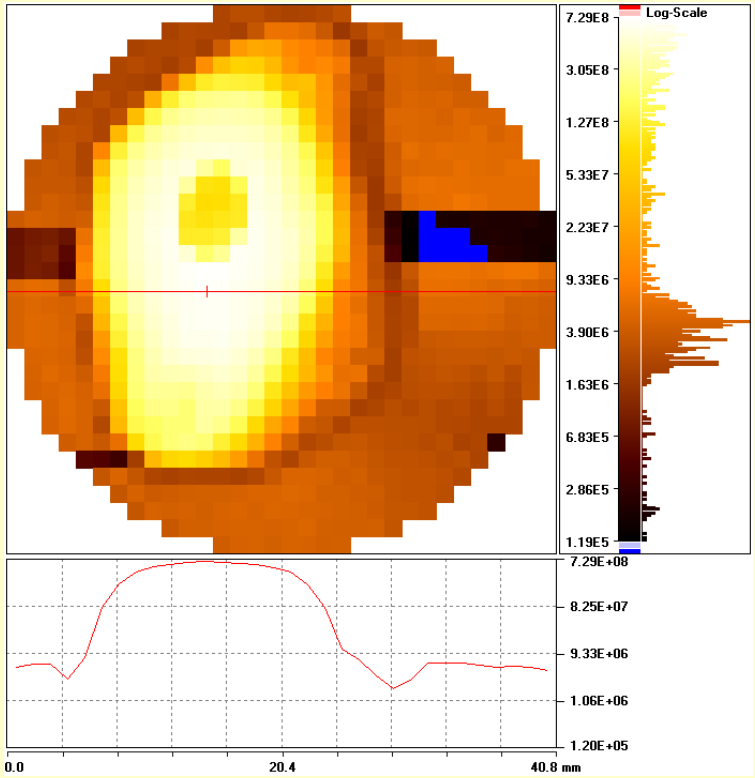
Resistivity Topography (V)

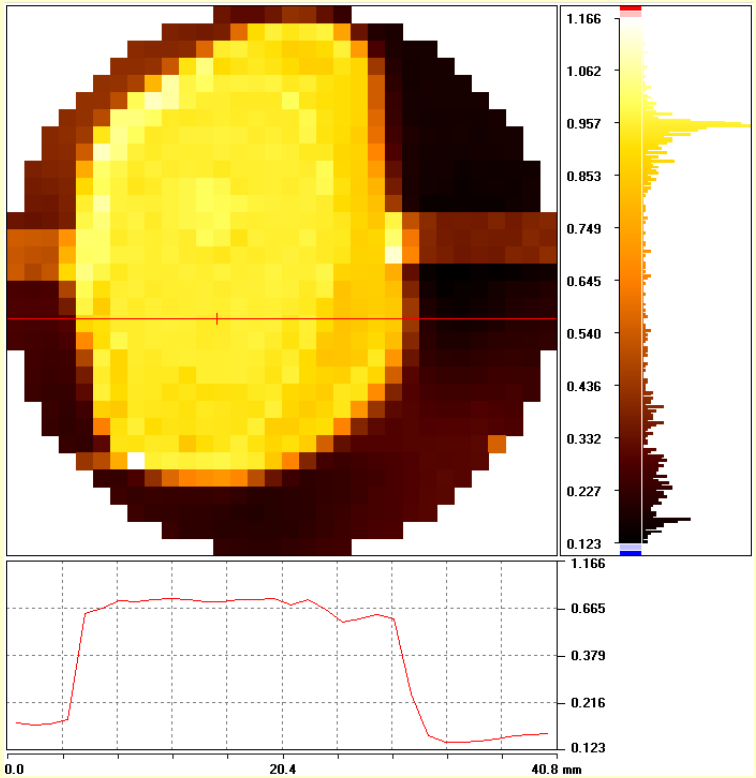
Analysis of locally inhomogeneous Material

Resistivity



Mean: 1.13 x10^8 Ωcm
Stdv: 168 %

Volume



Mean: 62%
Stdv: 54%

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Contactless Mobility Measurement (I)

	CONVENTIONAL HALL	COREMA - RM
Wafer cutting	necessary	nondestructive
Ohmic contacts	needed, critical	obsolete
Sample preparation	~ 15 min	none
Sample insertion and measurement time	~ 10 min	~ 30 s
Repeatability	~ 5%	< 1%
Evaluation of SI material	difficult	easy
Applicability	general	SI material only $\mu > 1000\ cm^2/Vs$
Acceptance	standard method	new method

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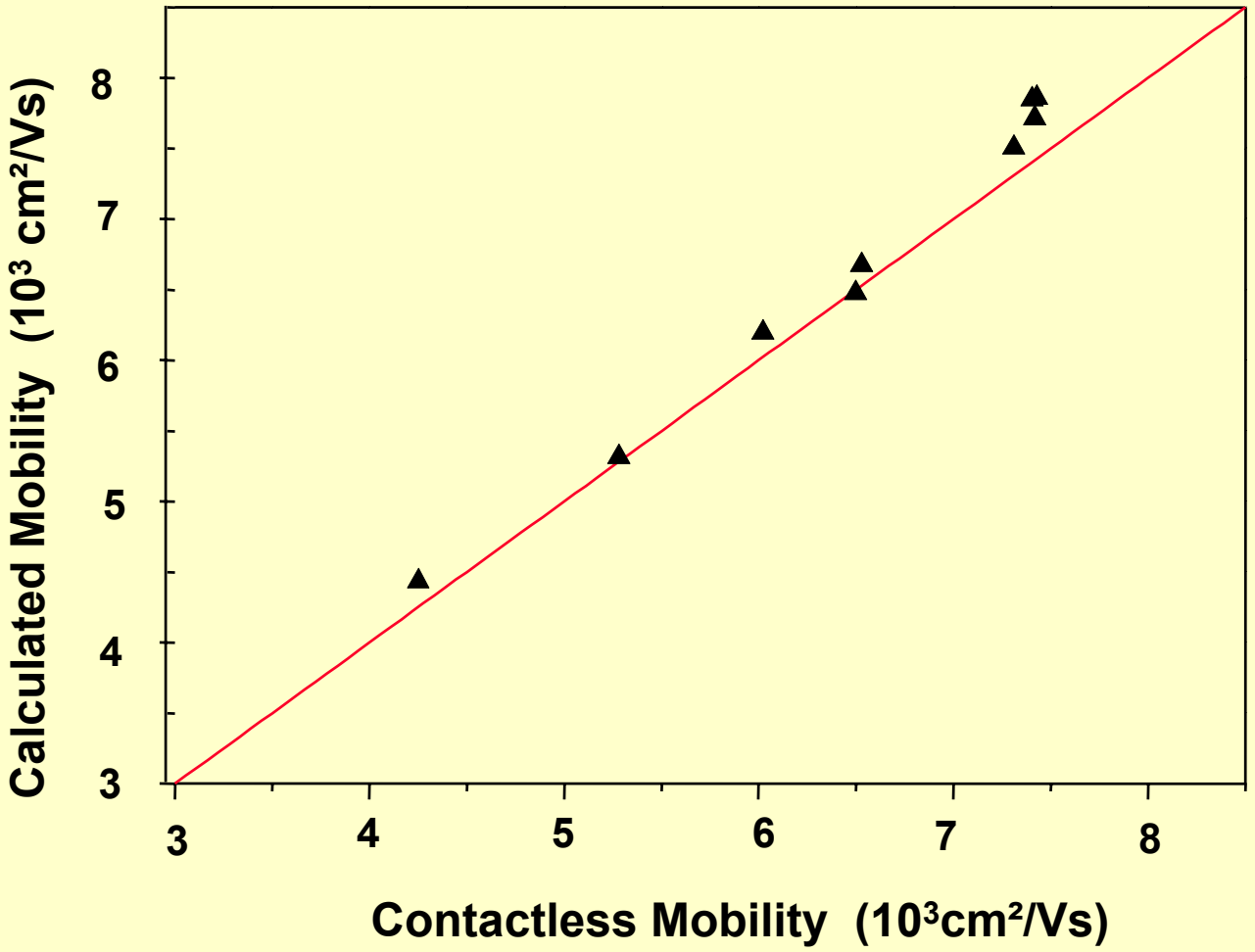
Contactless Mobility Measurement (II)

Verification using GaAs samples with different carbon content

Comparison with ionized impurity scattering theory



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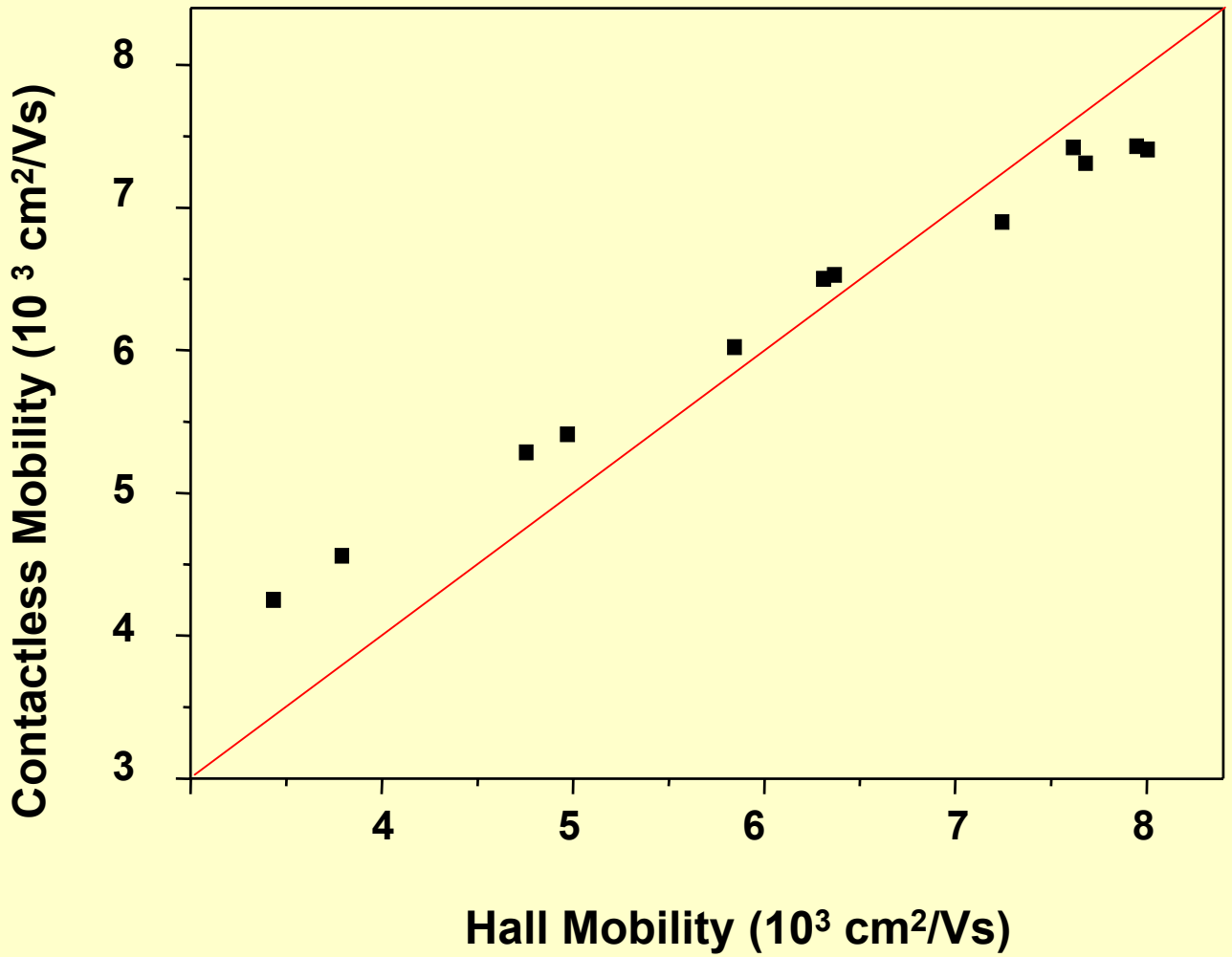
Contactless Mobility Measurement (III)

Verification using GaAs samples with different carbon content

Comparison with Hall data (sample size 27x27 mm²)



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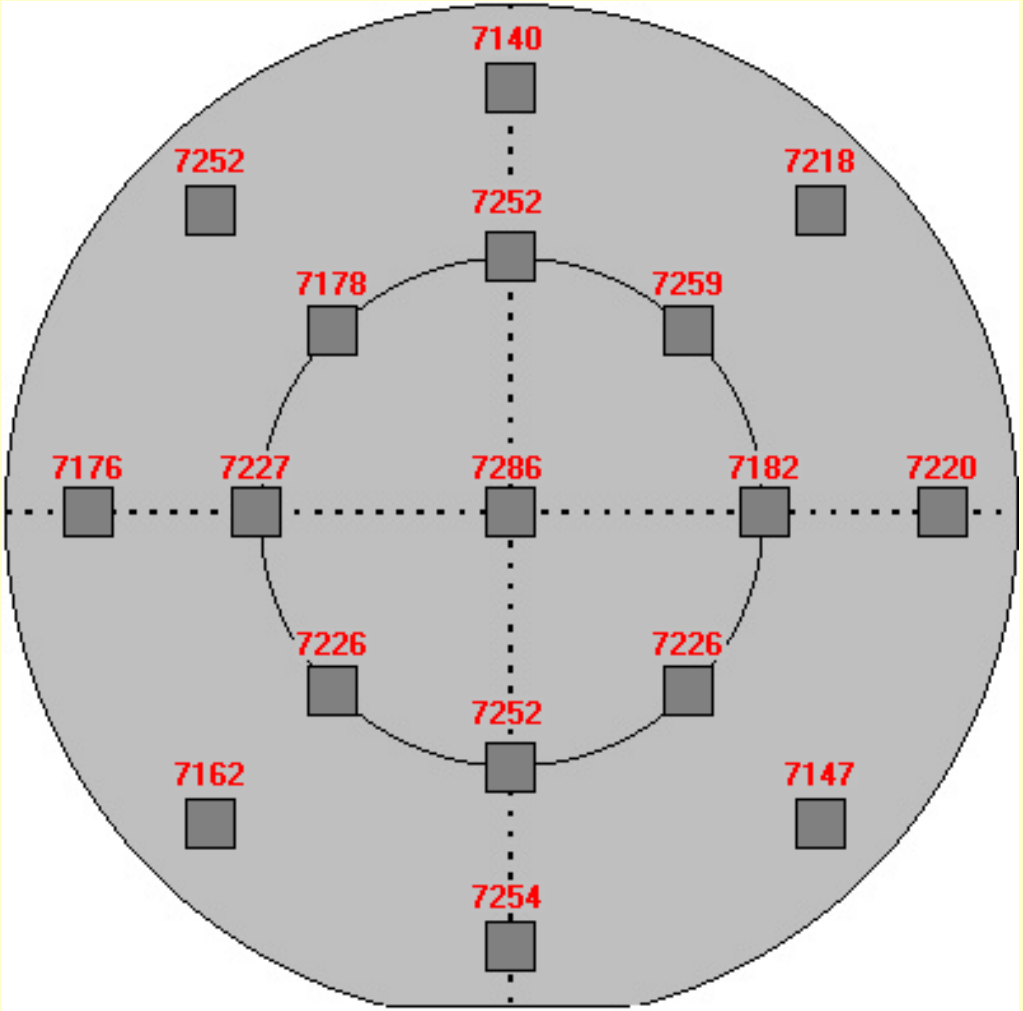
Contactless Mobility Measurement (IV)

Mobility evaluation using a customer specified measurement plan



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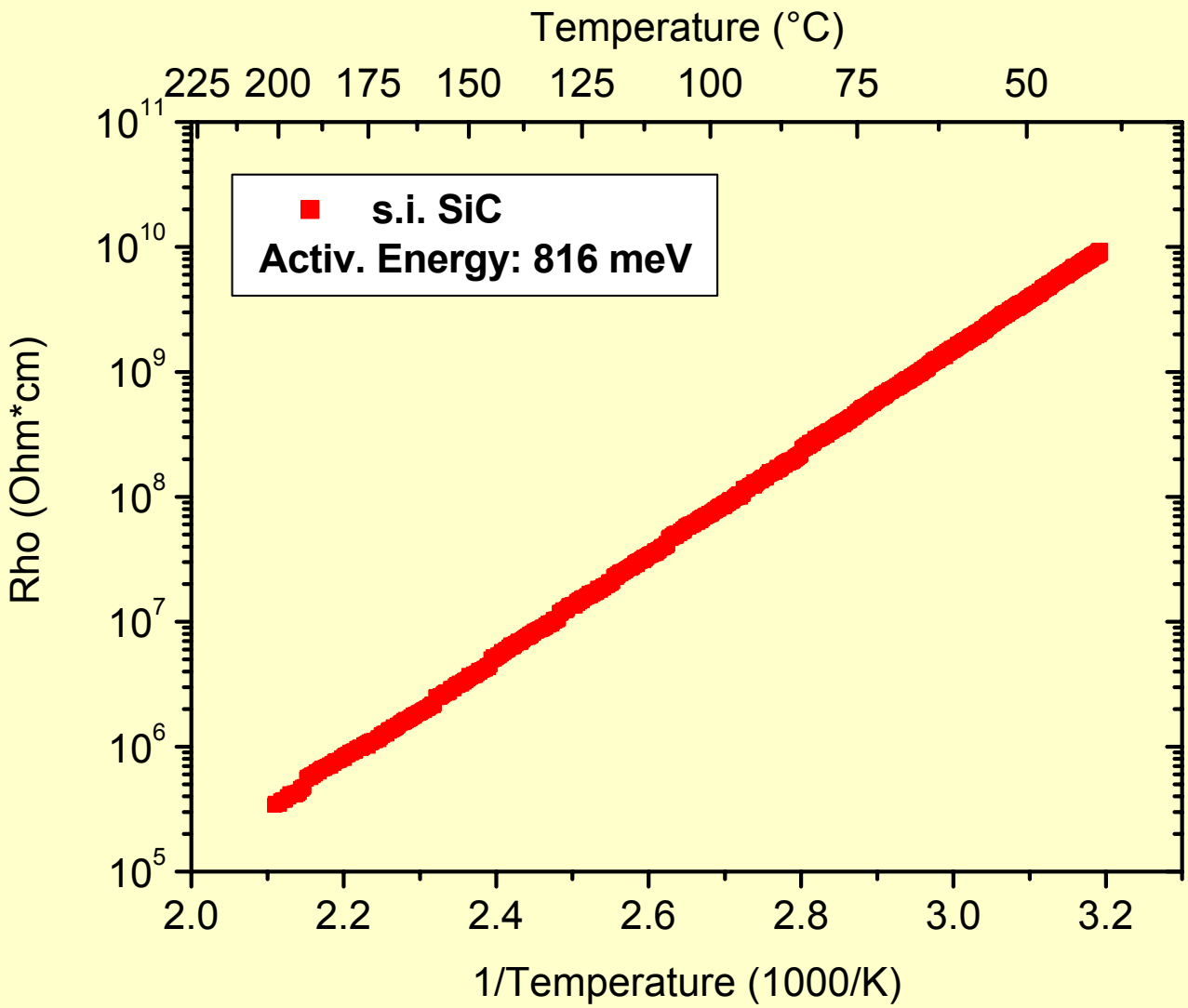
High Temperature Resistivity Measurement (I)

2“ SiC wafer

Temperature range
40 – 200 ^{0}C

Resistivity range
3x10^5 – 1x10^{10} Ωcm

Not semi-insulating
at 300 ^{0}C



$$E_a = (kT_1T_2)/(T_2-T_1) * \ln [\rho(T_1) / \rho(T_2)]$$

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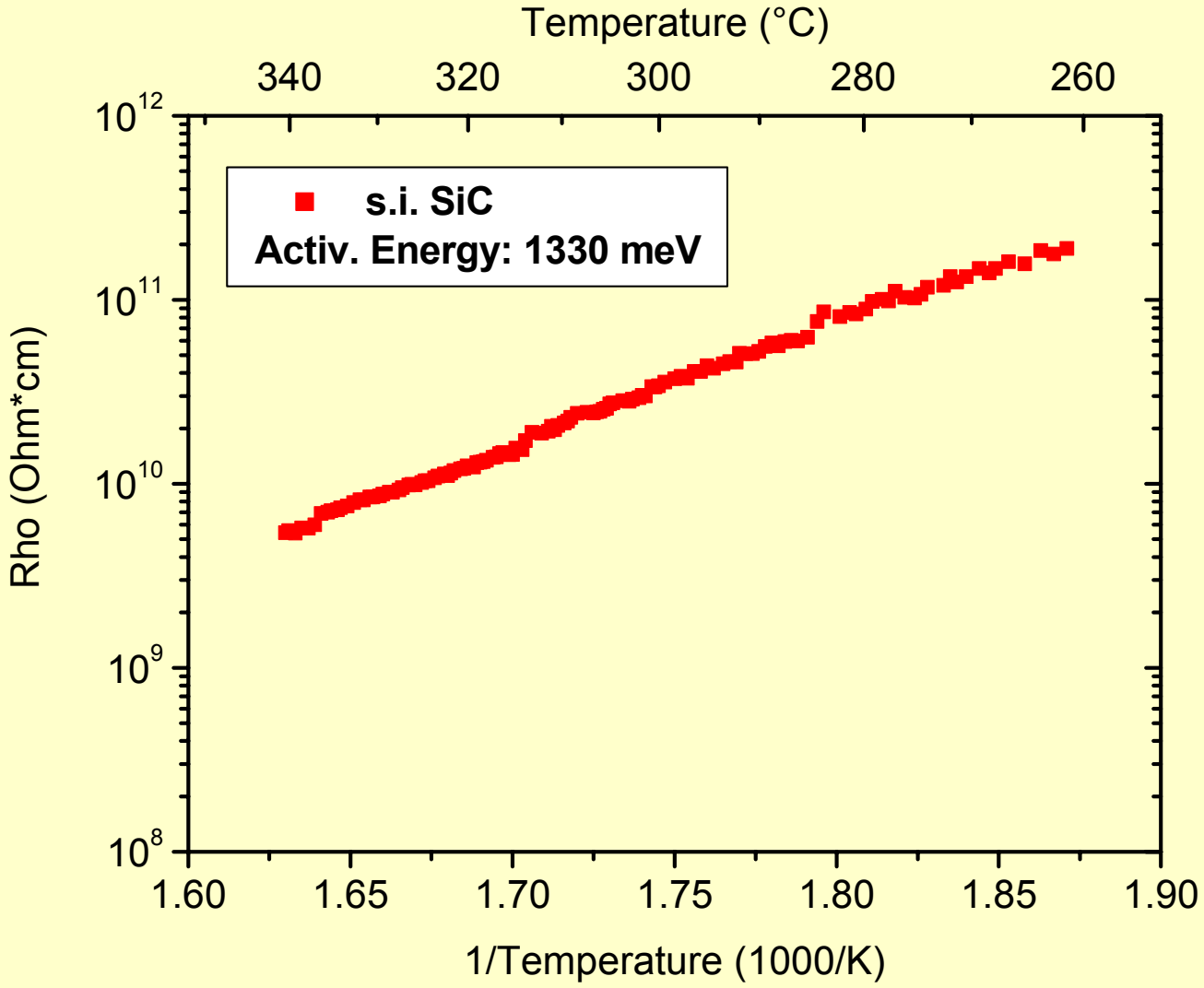
High Temperature Resistivity Measurement (II)

2“ SiC wafer

Temperature range
260 – 340 ^{0}C

Resistivity range
5.6 x10^9 – 1.8x10^{11} Ωcm

Semi-insulating at 300 ^{0}C



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High Temperature Resistivity Measurement (III)

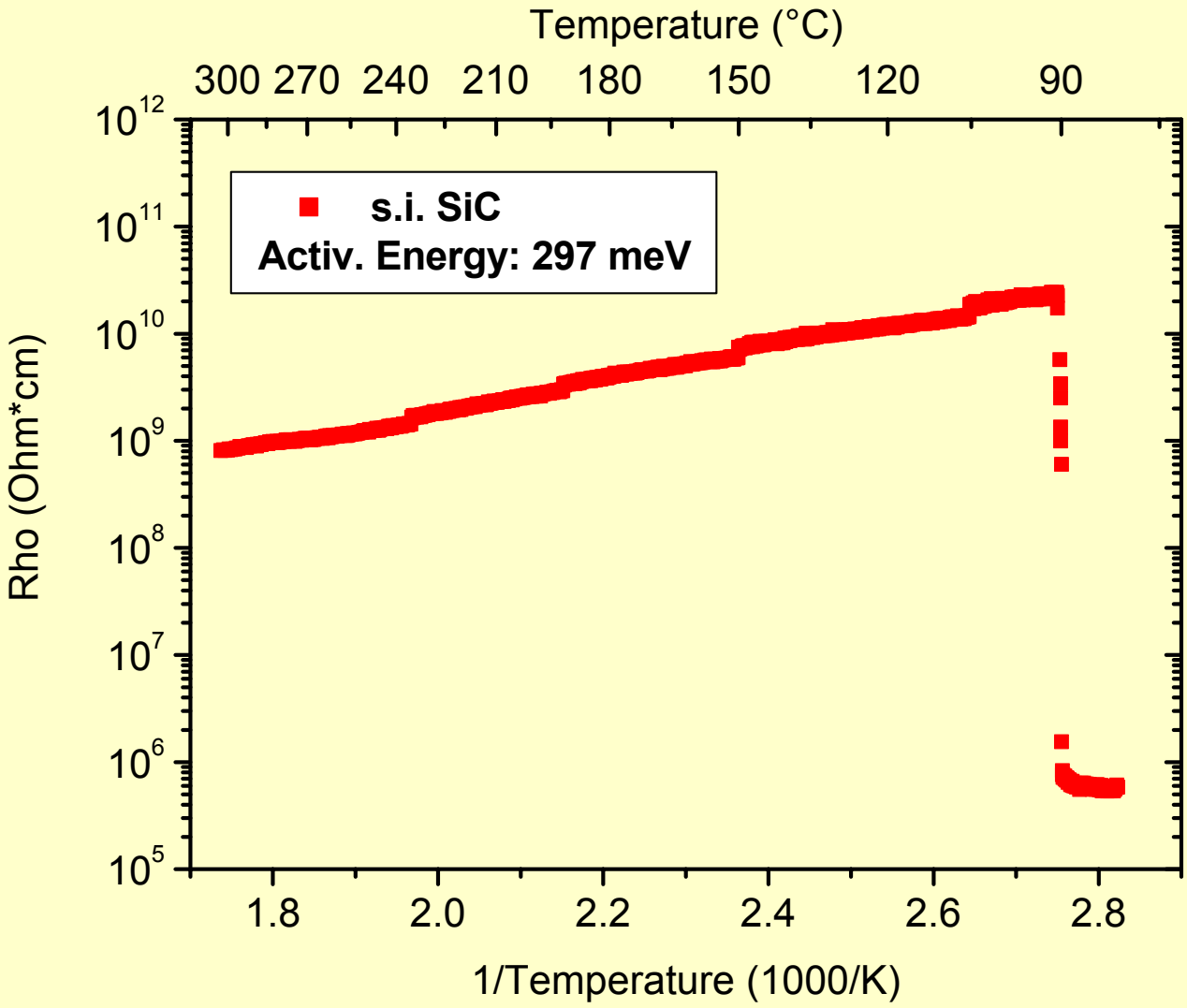
2“ SiC wafer

Temperature range
92 – 256 ^{0}C

Resistivity range
9.0 x10^8 – 2.3x10^{10} Ωcm

High resistivity, but small activation energy

Exhibits strong persistent photoconductivity



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Summary

- Automated resistivity topography is used extensively by industry and academia labs for routine wafer quality control and exploratory material analysis of GaAs, InP, SiC, CdT and GaN wafers.
- Mobility evaluation based on contactless magnetoresistance has been developed and commercially introduced for rapid, low-cost quality control of GaAs and InP wafers.
- A system measuring resistivity at temperatures up to 350 ^{0}C has been developed. The activation energy of state-of-the-art and exploratory SiC wafers has been obtained.

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