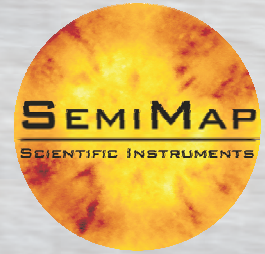


# Advanced Topographic Resistivity Analysis Of Semi-insulating SiC Substrates



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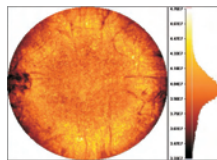
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## Outline

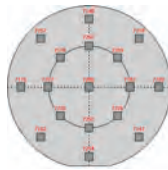
The growing complexity and maturity of SiC based high frequency, high power microelectronic devices and modules continually tightens the demand on the electrical quality of semi-insulating SiC substrates.

The topographic measurement system COREMA-WT and the temperature dependent measurement system COREMA-VT are used to characterize exploratory 40 mm diameter SiC wafers. We demonstrate that the combined analytic capabilities of these tools allow a very detailed assessment of the resistivity distribution across the entire wafer area. Both macroscopic variations, resulting from the growth process, as well as local intermixtures of material phases with different resistivities, resulting from incomplete compensation, are assessed with respect to absolute resistivity values and the respective volume contributions. We show that local inhomogeneity results in a temperature dependent activation energy.

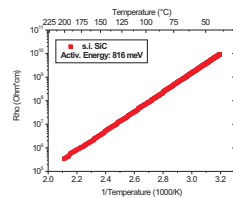
## COREMA System



**Resistivity Measurement**  
 150 mm GaAs wafer  
 Mean:  $3.96 \times 10^7 \text{ Ohm} \cdot \text{cm}$   
 Stdev: 4.3 %  
 Radial variation  
 Fourfold symmetry  
 Dislocation network



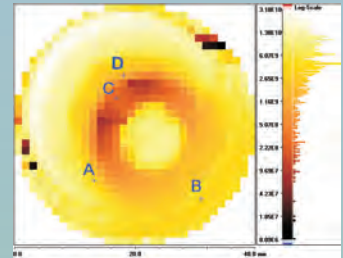
**Mobility Measurement**  
 Mobility measurement  
 150 mm GaAs wafer



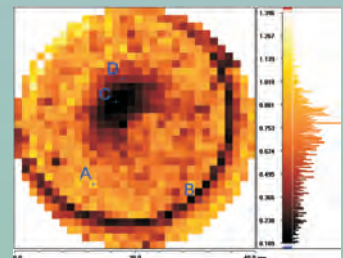
**Activation Energy**  
 2<sup>nd</sup> SiC wafer  
 Temperature range  
 40 – 200°C  
 Resistivity range  
 $3 \times 10^5 - 1 \times 10^{10} \text{ Ohm} \cdot \text{cm}$   
 Not semi-insulating at  
 300°C

## Resistivity

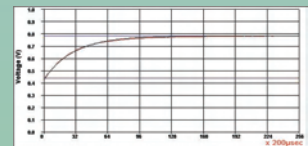
Resistivity Topogram



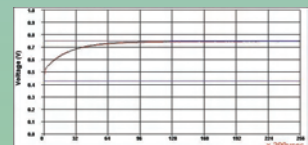
Volume Topogram



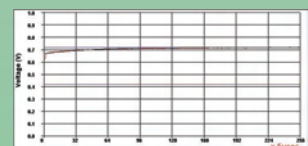
Position A, Volume = 100%



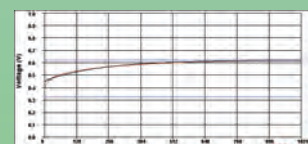
Position B, Volume = 58%



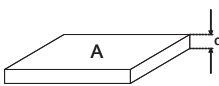
Position C, Volume = 10%



Position D, Volume = 50%



## Basics of Contactless Resistivity Mapping



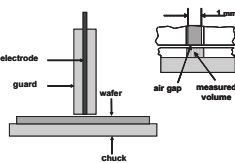
$$R_s = \rho d/A$$

$$C_s = \epsilon \epsilon_0 A/d$$

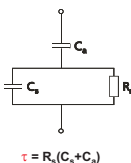
$$R_s C_s = \rho \epsilon \epsilon_0$$

Semi-insulating semiconductor

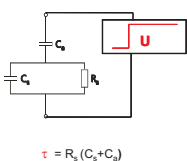
Capacitive probe



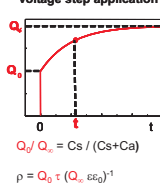
Equivalent circuit



Equivalent circuit



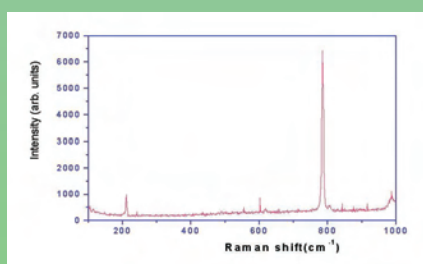
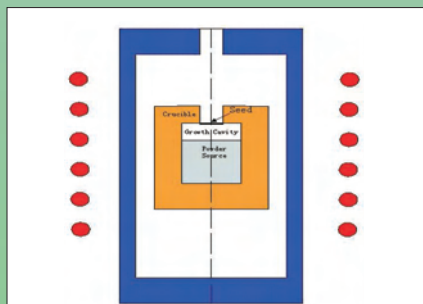
Charge transient after voltage step application



## Evaluation of electrical material properties

**Resistivity**  $\rho = Q_0 \tau / (Q_\infty \epsilon \epsilon_0)^{-1}$   
**Mobility**  $\mu = 1/B [ \rho(B) / \rho(0) - 1 ]^{-1/2}$   
**Activation energy**  $E_a = (kT_1 T_2) / (T_2 - T_1) * \ln [ \rho(T_1) / \rho(T_2) ]$

## S.i. SiC Crystal Growth



## Activation Energy

