

PVT Growth of P-Type and Semi-Insulating 2 Inch 6H-SiC Crystals

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Abstract P-type and semi-insulating 2" 6H-SiC crystals exhibiting very low resistivity inhomogeneities are demonstrated. Resistivity mappings of Aluminium-doped SiC-wafers reveal a lateral mean deviation of only 5 % and an axial variation of 30 %. Room temperature mappings of Vanadium-doped SiC-wafers exhibit a resistivity of $3 \times 10^{11} \Omega\text{cm}$ with a lateral mean deviation below 13 %.

Introduction Silicon carbide based electronic devices operating at high frequencies and elevated temperatures require high resistivity SiC substrates to reduce dielectric losses and device parasitics. Semi-insulating electrical properties of SiC single crystals can be achieved by the formation of deep level states in the band gap, either by

- (i) incorporation of suitable doping elements during crystal growth [1, 2, 3], or by
- (ii) reduction of residual impurities until intrinsic defects with appropriate electronic levels prevail [4, 5].

Both concepts are presently under discussion: some studies have suggested that negative parasitic effects in high frequency devices originate in vanadium traps and favoured high purity semi-insulating substrates (ii) instead [6], while others have focused on the surface passivation to control the density of surface states [7]. In this work, we applied the concept of intentional doping (i) because extrinsic defect centres are well known, temperature stable and can be introduced in a controlled and effective manner.

Theory Ideal high resistivity values are reached if energy states near the middle of the band gap are activated. Vanadium can act as an amphoteric deep level impurity, introducing two levels in the bandgap depending on the compensation mechanism:

- (i) Compensating residual nitrogen Vanadium forms an acceptor level A^-/A^0 ($V^{4+}/3+$) located at approximately $E_V + 0.8 \text{ eV}$ in 6H-SiC, resulting in a room temperature resistivity in the range of $10^{11} \Omega\text{cm}$ [3].
- (ii) As proposed by Schneider *et al.* [8], Vanadium compensating a shallow acceptor can be utilised as a deep donor which forms a deep-donor level D^0/D^+ ($V^{4+}/5+$) located at approximately $E_V + 1.5 \text{ eV}$ in 6H-SiC, resulting in a room temperature resistivity in the range of $10^{15} \Omega\text{cm}$ [1]. But, since the donor nitrogen is the dominating residual impurity in undoped PVT-grown SiC-crystals [9], it is necessary to overcompensate it simultaneously with a shallow acceptor.

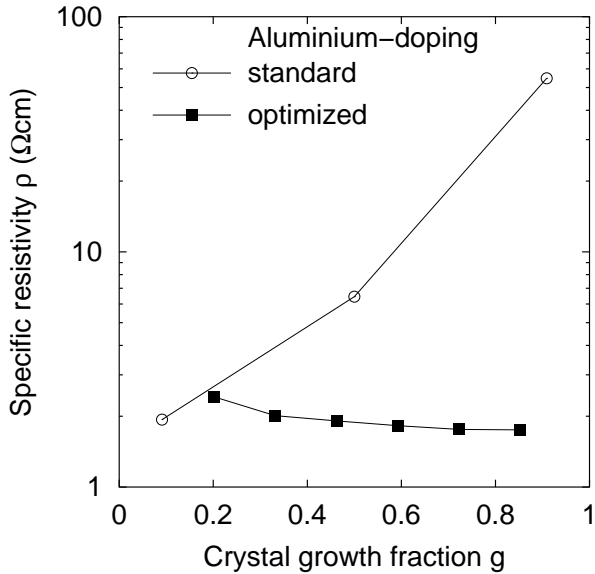


Figure 1: Dependence of mean resistivity of Aluminium-doped 2'' 6H-SiC wafers on growth time. In comparison to an unoptimised doping technique the optimised process markedly reduces the axial variation of resistivity below 30 %.

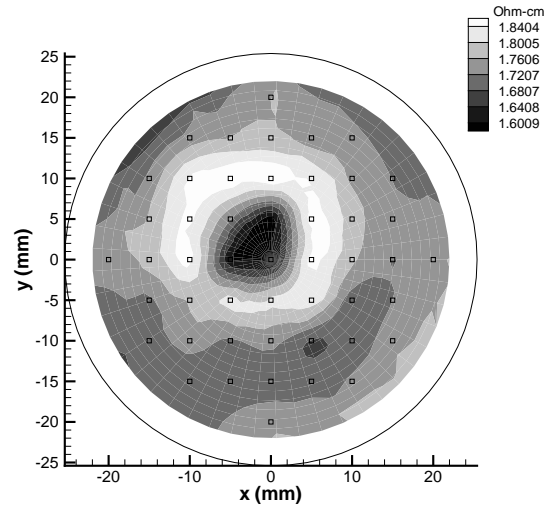


Figure 2: Resistivity mapping (units: Ωcm) of a Aluminium doped 6H-2''-SiC wafer at room temperature, obtained by four-point-probe technique. The mean resistivity is 1.7 Ωcm with a lateral mean deviation below 5 %.

Experiments Growth experiments were performed utilising the PVT-method, modified in order to introduce dopant atoms in a controlled manner during the entire growth run. The Aluminium and the Vanadium sources could be affected separately in order to manage a strict control over dopant incorporation during the entire growth time. Since the resulting resistivity of greater than 10^{14} Ωcm at room temperature is inaccessible to electrical characterisation, in this study the axial and lateral uniformity will be demonstrated separately for each doping system.

Wafers and samples were studied using GDMS analysis, resistivity mapping methods at room temperature (four-point-probe technique for p -type SiC and Compona measurement system (REF) for semi-insulating SiC), temperature-dependent Hall-effect measurements, and low-temperature photoluminescence measurement.

Results and discussion The Aluminium- and Vanadium-doped 6H-SiC crystals are of 2'' diameter and exhibit p -type and semi-insulating electrical properties, respectively. In applying the optimised doping techniques to our experimental set-up 6H-SiC crystals with very low axial and lateral doping inhomogeneities were grown. The crystalline quality was not affected as long as the dopant concentration was below its solution limit.

Axial uniformity In comparison to an unoptimised doping technique the optimised process markedly reduces the axial variation of resistivity (fig. 1). A simple addition of elemental Aluminium to the SiC source material results in a continual depletion of the dopant source and in a rapid increase of resistivity with growth time in nearly two orders of magnitude, whereas in the present study the axial variation could be reduced below 30 %. The slight decrease of resistivity can be traced back to a decrease of the nitrogen residual concentration which leads to a lower compensation ratio.

Lateral uniformity The lateral doping uniformity can be afflicted by several effects: growth surface effects (faceted and smooth interfaces), temperature differences, or the curvature of the phase boundary in combination with variable time-dependent impurity incorporation. By optimisation of

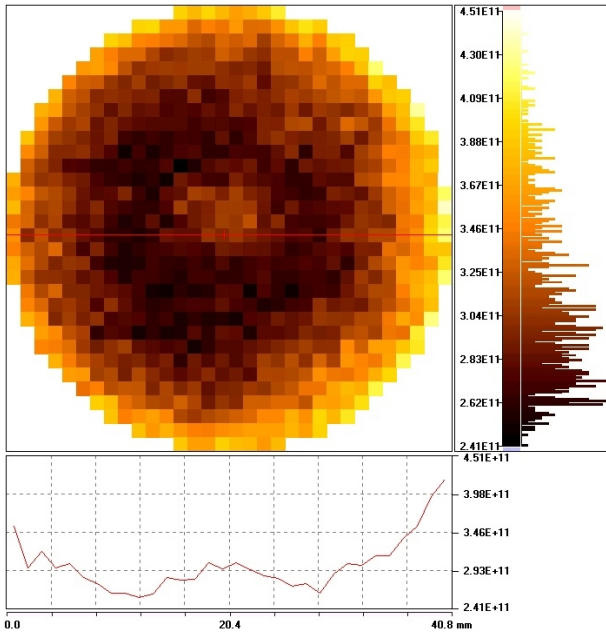


Figure 3: Resistivity mapping (units: Ωcm) of a Vanadium-doped 6H-2''-SiC wafer at room temperature. The mean resistivity is at $3 \times 10^{11} \Omega\text{cm}$ with a lateral mean deviation below 13 %.

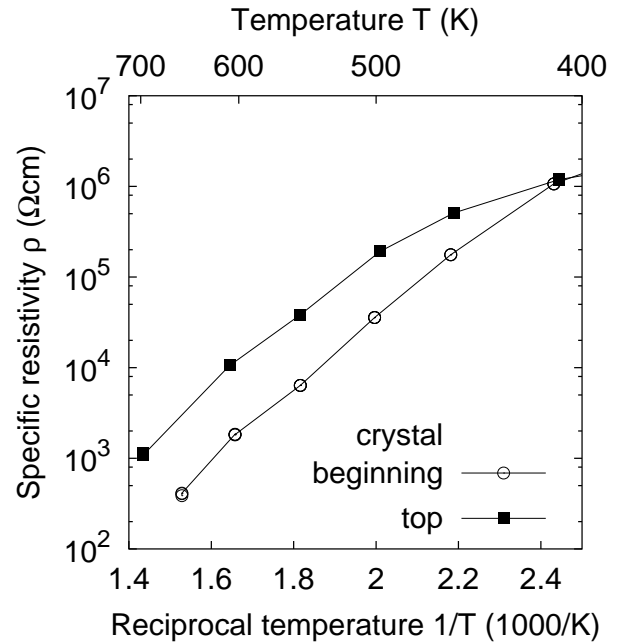


Figure 4: Temperature-dependent measurement of resistivity of Vanadium-doped 6H-SiC, revealing a trap activation energy of about 0.76 eV for both the first and the last wafer of the crystal.

the growth process we minimised the lateral doping inhomogeneities. The results of spatially resolved electrical characterisation of Aluminium- and Vanadium-doped SiC-wafers are shown in fig. 2 and fig. 3.

Room temperature resistivity mapping of Aluminium-doped SiC-wafers exhibits typically a lateral mean deviation of 5 %. The faceted growth region in the wafer centre yields lower resistivity due to an increased dopant incorporation there.

The measurement system Compona allows to . . . up to $10^{14} \Omega\text{cm}$. Fig. 3 shows a spatially resolved mapping of a Vanadium-doped SiC-wafer at room temperature revealing a resistivity of $3 \times 10^{11} \Omega\text{cm}$ with a lateral mean deviation below 13 % and a minimum value of $2.4 \times 10^{11} \Omega\text{cm}$.

The temperature-dependent measurement of resistivity of Vanadium-doped samples (fig. 4) reveals a trap activation energy of about 0.76 eV for both the first and the last wafer of the crystal, indicating that the whole boule is semi-insulating.

Optical characterisation IR photoluminescence and transmission spectroscopy experiments were performed on Vanadium-doped samples. Fig. 5 shows the resulting LTPL spectrum with lines characteristic for V^{4+} at 1309, 1350, and 1388 nm [10]. The peaks are strongly overdriven due to the high emission. At higher wave lengths lines appear which probably trace back to intrinsic defects. All wafers of the doped crystals were free of precipitates detectable by optical microscopy.

Conclusion In applying a sophisticated doping technique to SiC PVT growth it was possible to demonstrate *p*-type and semi-insulating 2'' 6H-SiC wafers exhibiting very low lateral resistivity inhomogeneities. A combination of strictly controlled Aluminium and Vanadium incorporation will allow the co-doping of SiC bulk crystals resulting in even higher resistivities. Only slight modifications have to be made for an adaptation of the doping method to the growth of 4H-SiC. In addition, impurity concentrations have to be reduced to fulfil requirements of crystalline perfection and device characteristics.

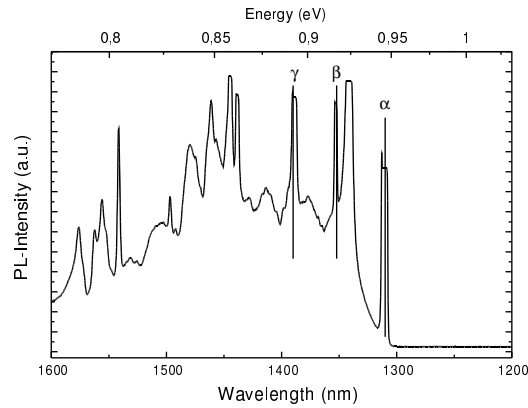


Figure 5: Low temperature photoluminescence measurement of a vanadium doped sample. In the infrared lines characteristic for V^{4+} can be found. At higher wave lengths lines appear which probably trace back to intrinsic defects.

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