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Nondestructive topographic resistivity evaluation of semi-insulating SiC substrates

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Semi-insulating silicon carbide single crystals have been grown using high temperature chemical vapor deposition without vanadium doping. The resistivity of standard and exploratory 2″ diameter substrates has been analysed topographically with 1 mm lateral resolution with an improved contactless resistivity mapping technique. Absolute resistivity values are ranging from below 1×10^5 to above 1×10^{12} Ω cm. The lateral homogeneity of state-of-the-art material is very satisfactory, whereas strong localized inhomogeneities in exploratory materials underscore the decisive advantage of a nondestructive and topographic resistivity evaluation in supporting the optimization of the crystal growth procedure.

1. Introduction Semi-insulating silicon carbide (SI SiC) substrates with a resistivity ρ exceeding 10^5 Ω cm are required for the fabrication of SiC and III–N microwave devices with low RF losses and high power densities. Such substrates are used for homoepitaxial device structures (e.g. SiC MESFETs) and, owing to the high thermal conductivity of SiC, are also advantageous for GaN/GaAlN/GaInN heteroepitaxial device structures. The SI property of SiC substrates is obtained by compensating the residual shallow donors and acceptors, such that the Fermi level is pinned at a partially ionized deep defect. The absolute values of the resulting ρ strongly depend on the starting materials and the crystal growth procedures and may vary from crystal to crystal, but also within a given crystal, in a wide range from below 10^5 to above 10^{12} Ω cm. Efficient electrical characterization, allowing to measure ρ accurately, rapidly and with high lateral resolution, is needed to optimize and control the growth procedure. A nondestructive approach is advantageous to avoid the time delay and uncertainty caused by sample preparation, but also the loss of expensive substrate material.

We show that the capacitive contactless resistivity mapping technique (COREMA) [1], which has successfully been established as a highly efficient evaluation tool for SI GaAs and InP substrates, can be upgraded to generate precise ρ topograms of SI SiC. The test measurements presented below include full wafer assessment of state-of-the-art homogeneous SI substrate material, but also show that strong inhomogeneities may occur, both on a macroscopic scale and at localized spots. These results underscore that full wafer topographic evaluation is needed for routine, comprehensive material control as well as detailed evaluation of exploratory material to support further growth process improvements.

2. Crystal growth procedure Vanadium doping of crystals grown by conventional physical vapor transport (PVT) has until recently been the method of choice for the fabrication of SI SiC substrates.

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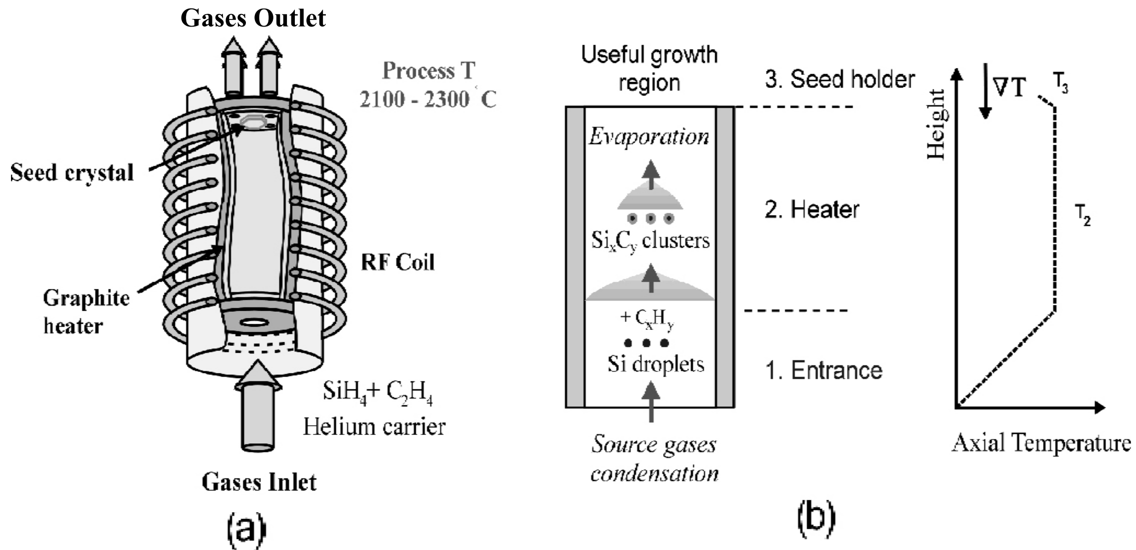

Fig. 1 a) Reactor geometry and b) growth species supply mechanism with the associated axial temperature distribution in the HTCVD process.

However, the performance of SiC MESFET devices processed on such wafers is generally limited by parasitic trapping effects related to a high concentration of impurities in the underlying substrate. We use high temperature chemical vapor deposition (HTCVD) to grow high purity SI SiC crystals. This method uses a vertical open reactor operating at temperatures above 2000 °C (Fig. 1a). The Si and C source material is provided by the gas precursors silane and ethylene, diluted in He carrier gas. Si_x clusters are formed at the entrance of the hot zone by thermal decomposition of silane (Fig. 1b). They interact chemically with C_2H_4 or its by-products, generating a mixture of Si_x–C_y clusters. This mixture passes through a high temperature zone where the clusters evaporate, such that a phase containing silicon and carbon vapor is generated. This vapor crystallizes at the SiC seed crystal, which is held at a lower temperature. HTCVD can be interpreted as "gas-fed sublimation", where the source material is synthesized from pure gases and subsequently is dissociated into the active species that are transported by the carrier gas to the growing SiC crystal.

3. Chemical analysis of SiC crystals The purity of the precursors used for HTCVD allows to grow vanadium-free SI 4H-SiC, as demonstrated in. Fig. 2. SIMS analysis corroborated that the V concentra-

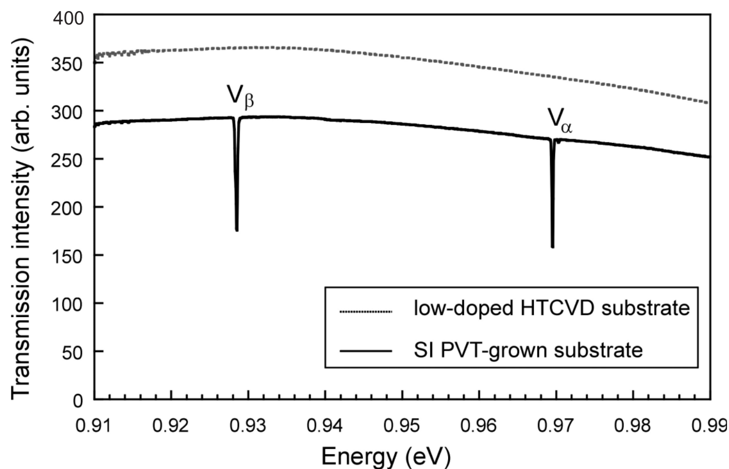

Fig. 2 Absorption spectra of a V doped PVT grown SI SiC substrate and a HTCVD grown SI 4H-SiC substrate of similar thickness. The absorption lines are due to the crystal field transitions of the neutral V^{4+} on the hexagonal (α) and cubic (β) lattice site [3].

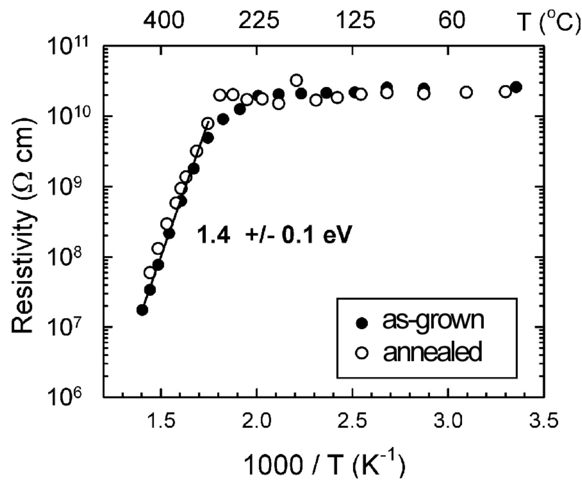

Fig. 3 Temperature dependent resistivity measurements of a sample containing the UD-1 center.

tion is below 5×10^{14} cm^{-3}. The concentration of shallow acceptors as Al is $<10^{14}$ cm^{-3} and of deep donors or deep acceptors below 10^{16} cm^{-3}. The nitrogen concentration is typically below SIMS detection limit and may also be as low as 10^{15} cm^{-3}.

It has been suggested that, instead of vanadium, the deep defect labeled UD-1 (unidentified defect 1), which is found in HTCVD grown SI 4H-SiC [2], serves to compensate shallow dopants. The UD-1 energy level is located approximately 1.4 eV within the band gap, as determined by photo-induced absorption measurements. This value agrees with the thermal activation energy obtained by temperature dependent resistivity measurements shown in Fig. 3. The resistivity does not change upon annealing at 1600 °C, which is the CVD growth temperature of MESFET structures.

4. Resistivity mapping The contactless resistivity mapping (COREMA) procedure [1, 4] is briefly reviewed here. Basically one measures the exponential decline, caused by the mobile carriers in the wafer material, of a voltage-induced dielectric polarization. Basically one measures the exponential decline, caused by the mobile carriers in the wafer material, of a voltage-induced dielectric polarization. The capacitive probe consists of a cylindrical metal stub, surrounded by a guard electrode, and a metal chuck which provides electrical back contact and mechanical support of the wafer to be measured (Fig. 4). The stub is approached to the wafer surface until the distance equals about 1/10 of the thickness of the wafer (Fig. 4, insert). A precise horizontal xy stage serves to translate the wafer underneath the probe in order to generate a resistivity topogram. The equivalent circuit of the arrangement (Fig. 5, insert) consists of the air capacitor of the spacing, the sample capacitor containing the portion of the wafer material below the stub and the shunt resistor representing the finite ρ of the wafer material.

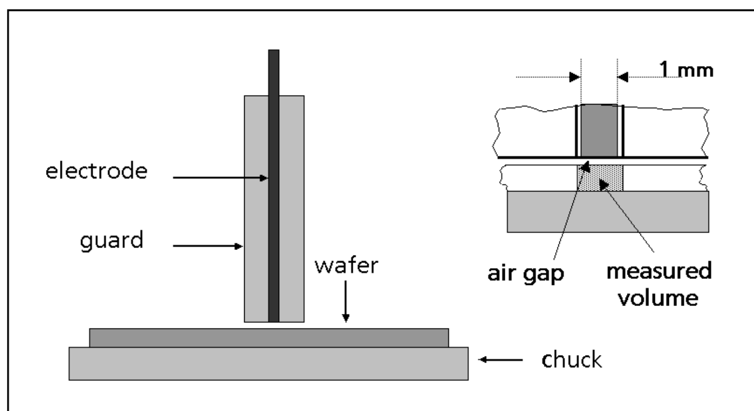

Fig. 4 Schematic representation of the COREMA measurement system. The blowup illustrates the details of the capacitive probe.

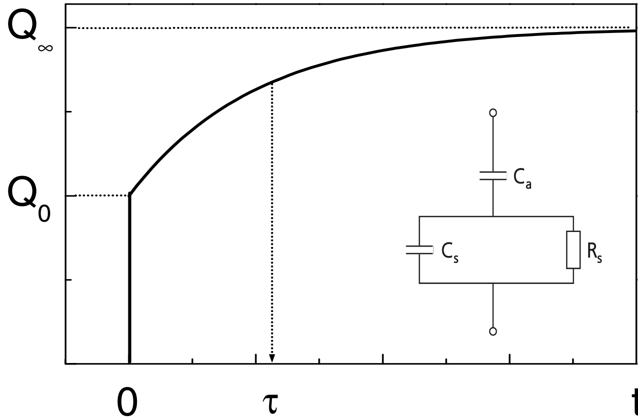

Fig. 5 Charge transient observed after application of a voltage step. The quantities needed to calculate ρ using Eq. (1) are indicated. The insert shows the equivalent circuit of the capacitive probe. The time scale depends on the resistivity (≈ 20 µs for $\rho = 10^7$ Ω cm).

The exponential time dependence of the charge $Q(t)$ shown in Fig. 5 allows to measure the relaxation constant τ and the charges $Q(0)$, $Q(\infty)$. Using these quantities and the dielectric constant ε, one obtains

$$\rho = \tau Q(0)/\varepsilon_0 \varepsilon Q(\infty) \,. \tag{1}$$

The capacitive evaluation does not require to cut samples and to prepare Ohmic contacts. It is very fast (100 ms for $\rho = 10^7$ Ω cm), highly repeatable (better than 1%) and yields topographic ρ images with high lateral resolution (≤1 mm). For these reasons, COREMA is superior to conventional contacting techniques, e.g. van der Pauw or linear four point probing.

Improvements of the COREMA measurement system for SiC evaluation include increased measurement range (10^6–10^9 Ω cm upgraded to 10^5–10^{12} Ω cm), automatic range switching for topographic measurement of highly inhomogeneous material, and software routines to evaluate locally inhomogeneous material, as shall be discussed below. The measurements were done at room temperature. Sometimes, a slow drift was observed, due to persistent photoconductivity. In such cases, the wafer was stored overnight in the dark and then measured in the dark.

5. Resistivity topograms SiC substrates cut from material with a high temperature resistivity as shown in Fig. 3 should be virtually isolating at room temperature. Indeed, wafers exhibiting above range resistivity ($\rho > 10^{12}$ Ω cm) across the entire wafer have been measured. While such topograms (not shown) may appear somewhat trivial, they are nevertheless most valuable, corroborating that indeed the full wafer area does exhibit very high resistivity.

Figures 6a, b show typical topograms of wafers with resistivities that are partially above, partially or fully within the measurement range $1 \times 10^5 - 1 \times 10^{12}$ Ω cm. The ρ distribution is further visualized by histograms. Pink color indicates $\rho > 10^{12}$ Ω cm. The topograms confirm that the respective wafers are cut from state-of-the-art material and meet the SI specification across the entire substrate area. In addition to this very comprehensive quality assessment the ρ images reveals informative features, such as radial symmetric dependencies and localized variations. They are due to crystal structure modifications or impurity fluctuations, not to be discussed here in detail. The variations within the (a, b) topograms are confined to a range that is entirely above SI specification, therefore may be inconsequential for substrate specification and device processing. Nevertheless they are helpful for analyzing and improving the details of the crystal growth procedure and the resulting shallow and deep defect distributions.

Figure 6c shows a wafer which is partly below 1×10^5 Ω cm, as indicated by light blue color. This lower limit of the measurement range coincides with the ρ value defining SI SiC material. Hence, this wafer does not meet the SI specification. It is obvious that, depending on the size and localization of such below-range-areas, the spec violation may not be revealed if only one or some few points on the wafer are evaluated. Again the detailed information supplied by the ρ image gives additional clues towards improving the material homogeneity.

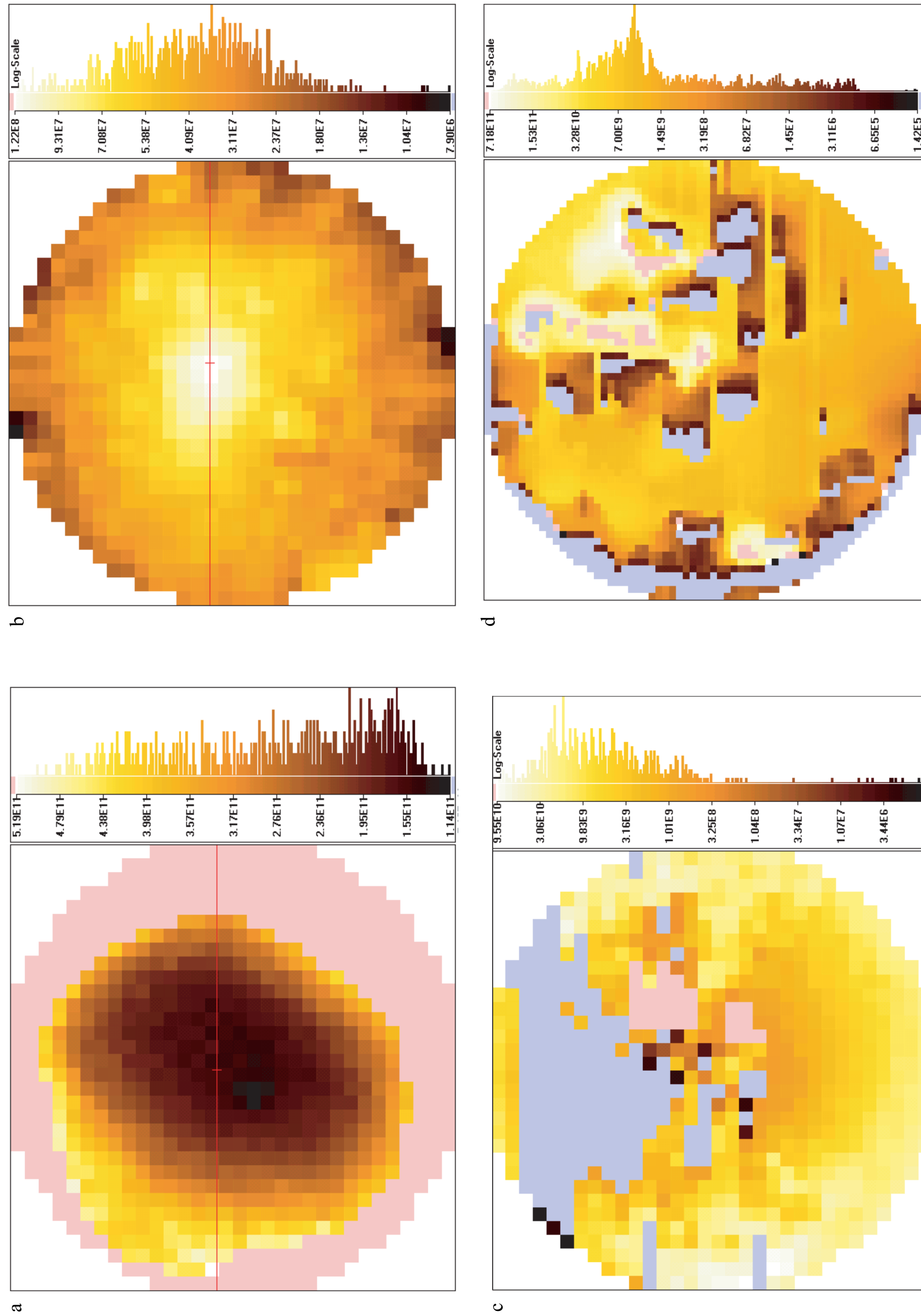

Fig. 6 Resistivity topograms of fully or partially semi-insulating SiC substrates. For details see text.

Finally, Fig. 6d depicts a wafer with localized, irregularly distributed below-range areas. This material, generated by an exploratory growth run, is shown here to demonstrate the capability of the COREMA technique in precisely analyzing highly inhomogeneous material. Evidently, in this case isolated data points, in particular if generated with conventional 10×10 mm^2 Hall samples, would be virtually meaningless.

6. Discussion The resistivity data presented above are covering a wide range of absolute values and exhibit very different variation patterns, including smooth macroscopic fluctuations as well as rapid order-of-magnitude changes within small distances. Such behavior is readily understood in terms of compensation processes. However, a simple model involving just one deep level, as tentatively suggested above, will not be sufficient to describe the large variety of data. Rather, it appears that the Fermi level may be pinned at different deep levels, depending on the local concentrations of shallow and deep defects.

Conventional contacting measurement techniques require that the material is homogeneous within the sample, or else yield an average value which may or may not be meaningful. A more detailed evaluation of the capacitive measurement, to be described in detail elsewhere, allows positive assessment whether the resistivity as obtained by evaluating the transient shown in Fig. 5 and is displayed in the topograms, is valid for the entire sample volume. If this is not the case, for instance if low resistivity inclusions are encountered within a high resistivity matrix, the percentage values of the respective volumes are given quantitatively. Since the sampled volume (a 500 µm thick, 1 mm ∅ disk) by itself is very small, submillimeter inhomogeneities may be revealed and analyzed. It is found that SI substrates as presented in Fig. 6a, b in general are also locally homogeneous. By contrast, the ρ values given in Fig. 6d mostly are valid for portions of the material only that may be as low as 10%, whereas the remainder of the material has below range resistivity. These observations again underscore that COREMA is indispensable for an adequate electrical characterization of SI SiC substrates.

7. Summary High purity SiC substrates are fabricated using the HTCVD process. SI behavior is achieved without vanadium doping. The resistivity is measured absolutely with a noncontacting capacitive probe in the range 10^5–10^{12} Ω cm. High resolution topographic images of the resistivity distribution are obtained. The results confirm state-of-the-art SI quality of standard wafers. Lateral inhomogeneities of exploratory material can be analyzed in detail. The wide range of absolute resistivity values and the variety of fluctuation patterns suggest strong variations of the residual impurity concentrations and the existence of different deep acceptor levels. Preliminary observations indicating sub-mm inhomogeneities are reported.

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